IN THE SPECIFICATION:

Please amend the specification by inserting the following paragraph and heading before line 3 on page 1:

--Cross-Reference to Related Applications

This is a division of Application Serial No. 09/845,466, filed April 30, 2001, which application is incorporated herein in its entirety by this reference.--.

Please modify the paragraph on page 7, lines 11-17, as indicated below:

Figure 4 is a block diagram of the exemplary embodiment of the memory implementation. This schematic is described with the logic shown ~~four~~ for the four 8-bit memories combined into two 16-bit structures. In this example, the size of the memory address, RMAL[14:0], runs from 14 to 0 just because of the size of the memory used in this example. The address size could be any number of bits, although at least three bits are needed in this embodiment to display the full structure allowing the lower two bits to select the correct block.

Please modify the paragraph on page 7, line 26, to page 8, line 4, as indicated below:

Consequently, the multiplex unit 423 receives both RMAL[14:0] and RMAL[14:2] increased by 1. If RMAL[1]*=1, that is RMAL[1]=0, RMAL[14:0] is supplied to OTP1 411 and OTP 0410. This is the case when logical address is a memory location stored in either OTP1 411 or OTP0 410. When RMAL[1]=1, corresponding to a logical address stored in either OTP3 413 or OTP2 412, RMAL[14:2] increased by 1 is supplied to Memory #2 402 and the row ~~form~~ from which OTP1 411 and OTP0 410 are read is shifted up by one. As this arrangement allows the data to be retrieved from two separate rows, where the row being accessed in OTP1 411 or OTP0 410 determined by RMAL[1], this arrangement can be referred to as "Dual Row Access (DRA)".